WHAT IS CLAIMED IS:

1. A thin film transistor substrate comprising:

an insulating substrate;

a first thin film transistor formed above said insulating substrate, wherein said first thin film transistor comprises a first active layer formed above said insulating substrate, a first gate insulating film formed on said first active layer, and a first gate electrode formed on said first gate insulating film; and

a second thin film transistor formed above said insulating substrate, wherein said second thin film transistor comprises a second active layer formed above said insulating substrate, and a second gate insulating film formed on said second active layer, a second gate electrode formed on said second gate insulating film,

wherein a thickness of said second gate insulating film is larger than a thickness of said first gate insulating film,

wherein said second active layer has at least two impurity doping regions which overlap said second gate electrode,

wherein said first active layer has at least two impurity doping regions formed in a self-aligning manner with respect to said first gate electrode, and

wherein said second gate electrode comprises a semiconductor layer.

2. The thin film transistor substrate according to claim 1,

wherein said second gate insulating film comprises said first insulating film and a gate cover film formed above said first gate insulating film.

3. The thin film transistor substrate according to claim 1,

wherein said impurity doping regions formed in a self-aligning manner are formed so as to overlap said first gate electrode by 0.1 μm or less.

4. The thin film transistor substrate according to claim 1,

wherein at least one of said impurity doping regions formed in a self-aligning manner with respect to said first gate electrode includes an LDD structure.

5. The thin film transistor substrate according to claim 1,

wherein said impurity doping regions which overlap said second gate electrode are formed so as to overlap said second gate electrode by 2.0 μm or less.

6. The thin film transistor substrate according to claim 1,

wherein at least one of said impurity doping regions which overlap said second gate electrode includes an LDD structure.

7. The thin film transistor substrate according to claim 1,

wherein said first gate electrode comprises a two-layer structure including a semiconductor layer and metal or metal silicide layer.

8. The thin film transistor substrate according to claim 1,

wherein said second gate electrode comprises a two-layer structure including a semiconductor layer and a metal or a metal silicide layer.

9. The thin film transistor substrate according to claim 1,

wherein said second thin film transistor further comprises a third gate electrode formed between second active layer and said second gate electrode.

10. The thin film transistor substrate according to claim 2,

wherein said second thin film transistor further comprises a third gate electrode formed on said first gate insulating film.

11. A thin film transistor substrate comprising:

an insulating substrate;

a first thin film transistor formed above said insulating substrate, wherein said first thin film transistor comprises a first active layer formed above said insulating substrate, a first gate insulating film formed on said first active layer, and a first gate electrode formed on said first gate insulating film; and

a second thin film transistor formed above said insulating substrate, wherein said second thin film transistor comprises a second active layer formed above said insulating substrate, and a second gate insulating film formed on said second active layer, a second gate electrode formed on said second gate insulating film,

wherein a thickness of said second gate insulating film is larger than a thickness of said first gate insulating film,

wherein said second active layer has at least two impurity doping regions which overlap said second gate electrode,

wherein said first active layer has at least two impurity doping regions formed in a self-aligning manner with respect to said first gate electrode, and

wherein said second thin film transistor further comprises a third gate electrode formed between second active layer and said second gate electrode.

12. The thin film transistor substrate according to claim 11,

wherein said third gate electrode is formed of the same material as said first gate electrode, and

wherein said third gate electrode has the same thickness as said first gate electrode.

13. The thin film transistor substrate according to claim 11,

wherein said impurity doping regions formed in a self-aligning manner are formed so as to overlap said first gate electrode by 0.1 μm or less.

14. The thin film transistor substrate according to claim 11,

wherein at least one of said impurity doping regions formed in a self-aligning manner with respect to said first gate electrode includes an LDD structure.

15. The thin film transistor substrate according to claim 11,

wherein said impurity doping regions which overlap said second gate electrode is formed so as to overlap said second gate electrode by 2.0 μm or less.

16. The thin film transistor substrate according to claim 11,

wherein at least one of impurity doping regions which overlap said second gate electrode includes an LDD structure.

17. The thin film transistor substrate according to claim 11,

wherein said third gate electrode comprises a two-layer structure including a semiconductor layer and a metal or a metal silicide layer..

18. A method for manufacturing a thin film transistor substrate comprising:

providing an insulating substrate;

forming a first active layer above said insulating substrate;

forming a second active layer above said insulating substrate;

forming a first gate insulating film on said first active layer and on said second active layer;

forming a first gate electrode above said first active layer;

forming impurity doping regions in said first active layer by doping impurity, said impurity doping regions formed in a self-aligning manner with respect to said first gate electrode;

forming impurity doping regions in said second active layer by doping impurity;

forming a gate cover film above said first gate insulating film and said first gate electrode; and

forming a second gate electrode above said second active layer,

wherein said second gate electrode includes at least two portions, and each of said two portions overlaps each one of said impurity doping regions in said second active layer, and

wherein said second gate electrode includes at least a semiconductor layer.

19. The method for manufacturing a thin film transistor substrate according to claim 18,

wherein said semiconductor layer is deposited by plasma enhanced CVD method.

20. The method for manufacturing a thin film transistor substrate according to claim 18, further comprising:

forming a third gate electrode above said second active layer before forming said gate cover film.

21. The method for manufacturing a thin film transistor substrate according to claim 20,

wherein said third gate electrode is formed in the same step as said step of forming said first gate electrode.

22. The method for manufacturing a thin film transistor substrate according to claim 18, further comprising

activating said impurity doped into said impurity doping region in said first active layer and second active layer after said steps of forming impurity doping regions in said first active layer and said second active layer.

23. The method for manufacturing a thin film transistor substrate according to claim 22,

wherein said step of activating said impurity is performed by photoirradiation or a rapid heating method in which a heated gas is sprayed.

24. The method for manufacturing a thin film transistor substrate according to claim 18, further comprising

performing a hydrogenation process before said step of forming a second gate electrode.

25. The method for manufacturing a thin film transistor substrate according to claim 24,

wherein said hydrogenation process is performed once.

26. The method for manufacturing a thin film transistor substrate according to claim 18,

wherein said first gate electrode is formed by depositing a semiconductor thin film according to a plasma enhanced CVD method.

27. The method for manufacturing a thin film transistor substrate according to claim 18,

wherein said first gate electrode and said second gate electrode are formed by depositing metal or metal silicide after depositing a semiconductor thin film according to a plasma enhanced CVD method.

28. The method for manufacturing a thin film transistor substrate according to claim 18,

wherein said first active layer and said second active layer are formed in an island shape above said insulating substrate.